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Agilent no longer sells or supports this product. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available. You will find any other available product information on the Agilent Test & Measurement website, www.tm.agilent.com.

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

User's Guide

Publication Number E2470-97001
First Edition, February 1996

For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2470A MC68HC16Y1 Preprocessor Interface

The HP E2470A Preprocessor Interface—At a Glance

The HP E2470A Preprocessor Interface provides a complete interface for state or timing analysis between any Motorola MC68HC16Y1 target system and the following HP logic analyzers:

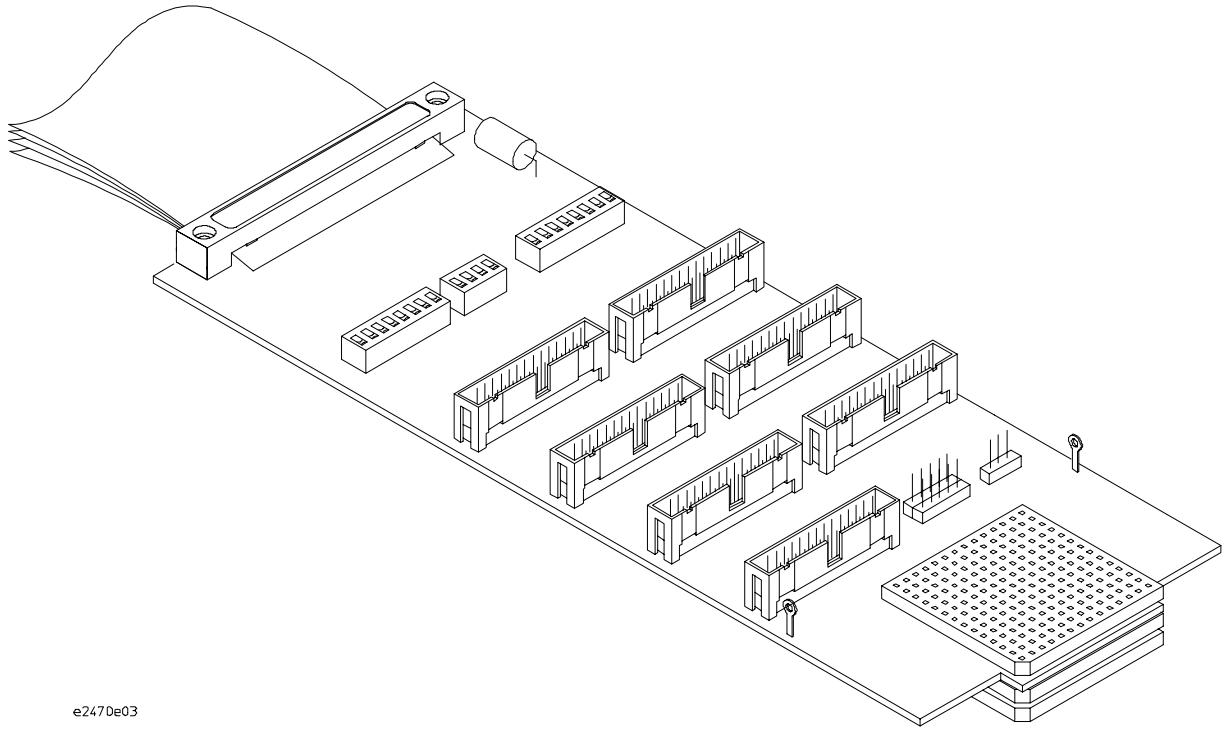
- HP 16550A (one-card)
- HP 16554A/55A/56A (one-card)
- HP 1660A/61A/62A
- HP 1660AS/61AS/62AS

For this preprocessor, two configuration files are provided for each analyzer: one for timing measurements and one for state measurements. These files allocate channels, label buses, and label individual signals according to the predefined format of the preprocessor connectors. For state measurements, an inverse assembler converts captured microcontroller instruction cycles into MC68HC16Y1 assembly language mnemonics.

The slide switches are used to inform the inverse assembler about the microcontroller configuration. The user must set these switches appropriately before making a state measurement.

The interface contains 13 connectors: 7 for timing measurements, 4 for state measurements, and 2 for the background debug monitor (BDM) interface. The timing connectors present raw microcontroller signals to the logic analyzer, while the state connectors present both raw and generated signals. The BDM interface provides easy connection for an external controller to view and alter microcontroller registers and system memory.

The HP E2470A is attached to the target system via an HP E5335A probe adapter.



HP E2470A Preprocessor Interface

In This Book

This book is the user's guide for the HP E2470A Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microcontroller being analyzed.

This user's guide is organized into three chapters:

Chapter 1 explains how to attach the preprocessor to the target and how to configure the logic analyzer for state and/or timing analysis.

Chapter 2 provides reference information on the format specification and symbols configured by the preprocessor interface software and information about the inverse assemblers and status encoding.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

For more information on the logic analyzers or microcontroller, refer to the appropriate reference manual for those products.

Contents

1

Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the HP E2470A Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers.

This section lists the logic analyzers supported by the HP E2470A and provides other information about the analyzers and the preprocessor interface.

Equipment Supplied

- The preprocessor interface circuit card.
- The configuration and inverse assembler software on a 3.5-inch disk.
- This User's Guide.

Minimum Equipment Required

- The HP E2470A preprocessor interface.
- The HP E5335A probe adapter.
- The configuration and inverse assembler software on a 3.5-inch disk.
- One of the logic analyzers listed in the following table:

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16550A (one card)	102	100 MHz	250 MHz	4 k states
16554A (one card)	68	70 MHz	125 MHz	512 k states
16555A (one card)	68	110 MHz	250 MHz	1 M states
16556A (one card)	68	100 MHz	200 MHz	1 M states
1660A/AS	136	100 MHz	250 MHz	4 k states
1661A/AS	102	100 MHz	250 MHz	4 k states
1662A/AS	68	100 MHz	250 MHz	4 k states

Setting Up the Preprocessor Interface Hardware

Setting up the preprocessor interface hardware consists of the following major steps:

- Turn off the logic analyzer and the target system.

CAUTION

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. Because the logic analyzer supplies power to the preprocessor interface, the logic analyzer should always be powered up before the target system; when powering down, power down the target system first and then power down the logic analyzer.

- Set the slide switches on the top of the preprocessor interface according to the configuration of the MC68HC16Y1.
- Attach the HP E5335A probe to the target system.
- Attach the preprocessor interface to the HP E5335A probe.
- Connect the logic analyzer pods to the cable connectors of the preprocessor interface board.
- Load the appropriate configuration file.

The remainder of this section describes these general steps in more detail.

To power up or power down

When powering up, the logic analyzer must be powered up first, followed by the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface. Unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, followed by the logic analyzer.

To protect the preprocessor interface when not in use

- **Cover the socket assembly pins of the preprocessor interface with a conductive foam wafer or conductive plastic pin protector.**

  The socket assembly pins of the preprocessor interface were covered at the time of shipment with either a conductive foam wafer or conductive pin protector. If this device is not damaged, it may be reused repeatedly.

- **Store the preprocessor interface in an antistatic bag or container.**

Electrostatic Discharge

The socket assembly pins of the preprocessor interface should be covered with a conductive foam wafer or pin protector to protect the delicate gold plated pins of the assembly from damage due to impact. Covering the pins and properly storing the preprocessor interface also protects the active circuitry on the preprocessor interface from electrostatic discharge.

To set the slide switches

The slide switches are used to inform the inverse assembler about the MCU configuration when making state measurements. The switches perform three functions. First, they validate a multi-function pin as an MCU signal versus a general purpose input/output for direct use by the inverse assembler. Second, they validate a multi-function pin as an MCU signal versus a general purpose input/output for use in generating signals to be used by the inverse assembler. Third, the slide switches direct the logic analyzer to capture bus cycles generated by other bus masters and/or debug controllers. They must be set appropriately for correct inverse assembly.

The overlay supplied with the preprocessor card labels the function of each switch and shows the position of valid and invalid settings. You may wish to refer to it as each switch is being discussed below.

Ten switches validate the chip select signals (CS0, CSM, CSE, CS3, CS5-10).

> Signals A19—A23 and CS6—CS10 are multiplexed onto the same pins, and the default configuration file for the logic analyzer assumes that signals A19—A23 are valid. If any of the chip selects, CS6—CS10, are being used and the appropriate switch(es) are set to VALID on the preprocessor, then the bits associated with A19—A23 should be removed from the ADDR label via the format menu in the logic analyzer. This corresponds to bits 3—7 of logic analyzer pod P4. This results in the display of correct address information in the ADDR field of the listing menu and presents only valid address bus bits to the ADDR field in the trigger menu.

- If the MC68HC16Y1 configuration is using any of the chip selects, set the associated switch to the VALID position. Set all others to the INVALID position.

  Six switches are used to validate control signals from the MCU. They are: SIZ0, SIZ1, DSACK0, DSACK1, AS, and DS.

> In order to distinguish between internal and external bus cycles, the preprocessor must have one of the following combinations: DS and AS must be valid or DS and at least one CS must be valid. If DS is the only valid control signal, all cycles will be interpreted as internal cycles.

Two switches are used to capture bus cycles not associated with the execution of user code. ACQNONMCU controls whether the logic analyzer acquires bus cycles caused by other bus masters in the target system (BGACK asserted). ACQBKGND controls whether the logic analyzer acquires bus cycles caused by a controller performing debug commands (FREEZE asserted).

- If the MC68HC16Y1 configuration is using BGACK and/or FREEZE and you want to capture these cycles, set the associated switch to the VALID position. Otherwise, set the associated switch to the INVALID position.

To connect to the target system

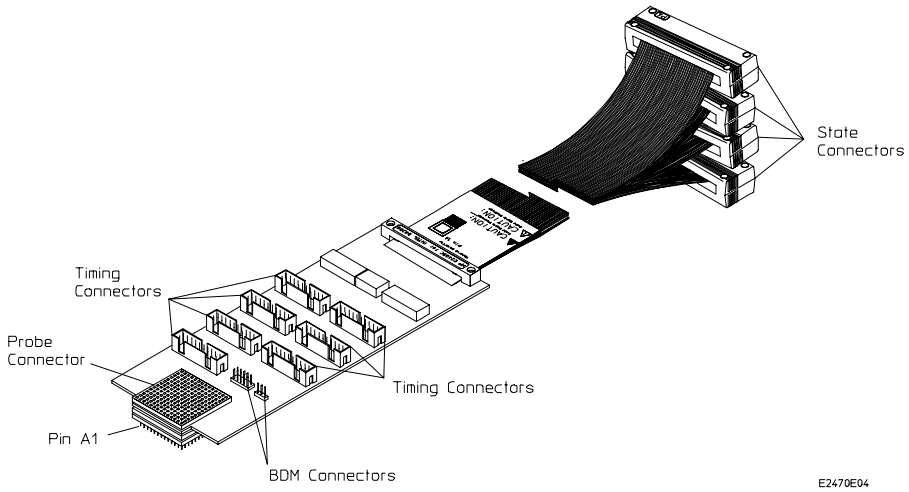
The preprocessor interface requires a probe adapter for connecting to the MC68HC16Y1 microcontroller. The probe adapter assembly allows the preprocessor interface to be connected without removing the microcontroller from the target system.

- To prevent equipment damage, remove power from both the logic analyzer and the target system.
- Using the instructions in the HP E5335A probe adapter manual, connect the probe adapter assembly to the target system microcontroller. Ensure that pin 1 is properly aligned.

CAUTION

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 and pin A1 on the preprocessor interface, probe adapter assembly, and microcontroller prior to making any connection. Also, take care to align the preprocessor interface connector with the pins on the probe adapter assembly so that all pins are making contact.

- Install the preprocessor interface into the PGA socket on the PQFP probe adapter. Again, ensure that pin A1 is properly aligned.



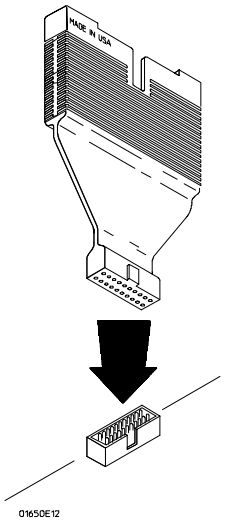
Preprocessor Interface Assembly

To connect the termination adapters

The logic analyzer probes must be terminated for correct operation.

The nonterminated connectors, P1 through P7, must be probed by using either the General Purpose probes (shipped with the logic analyzer) or the 100 kOhm Termination Adapters (HP part number 01650-63203).

- Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables. Push the termination adapter into the connector.
- Connect the female end of the termination adapter to the preprocessor interface.

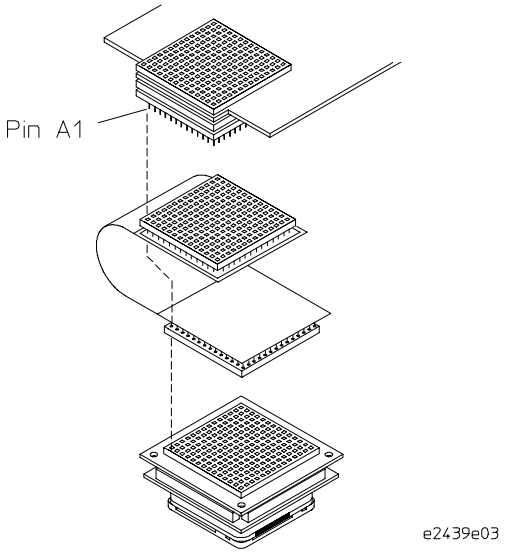


Connecting the Termination Adapter

Using the flex adapter

The HP E3445A flex adapter is designed to relieve mechanical stress and to provide a degree of freedom between the probe adapter and the preprocessor.

- Choose an orientation for the best physical arrangement of the preprocessor.
  The orientation will not affect electrical performance.
- Attach the flex adapter to the probe adapter.
- Fold the open end of the flex adapter onto itself.
  Note the location of Pin 1 on the microcontroller.
- Position and attach the preprocessor to the flex adapter aligning preprocessor pin A1 directly above the microcontroller pin 1.



Flex Adapter Diagram

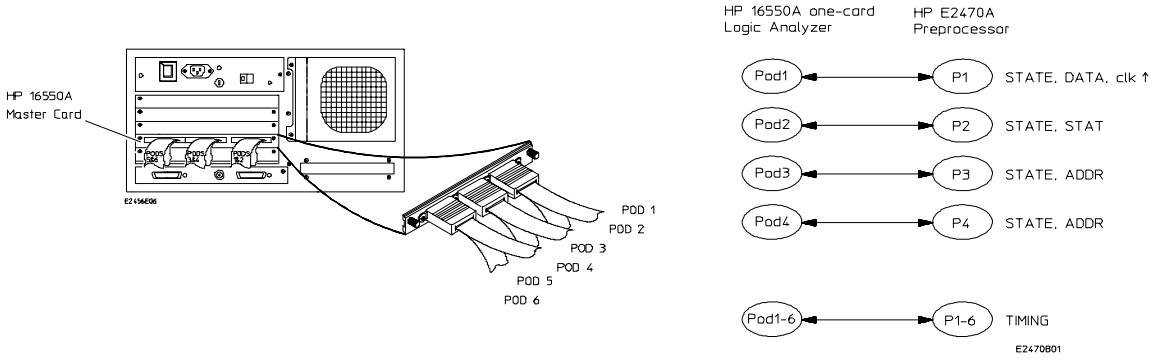
The flex adapter contains a 15 x 15 array of pins while the preprocessor contains only 14 x 14. When the flex adapter is folded over, there is a 1:1 correspondence between vertical pins. Be sure to attach the preprocessor to the appropriate set of pins attached to the target.

Connecting to the Logic Analyzer

Use the following tables and illustrations to connect the logic analyzer to the preprocessor interface.

To connect to the HP 16550A one-card analyzer

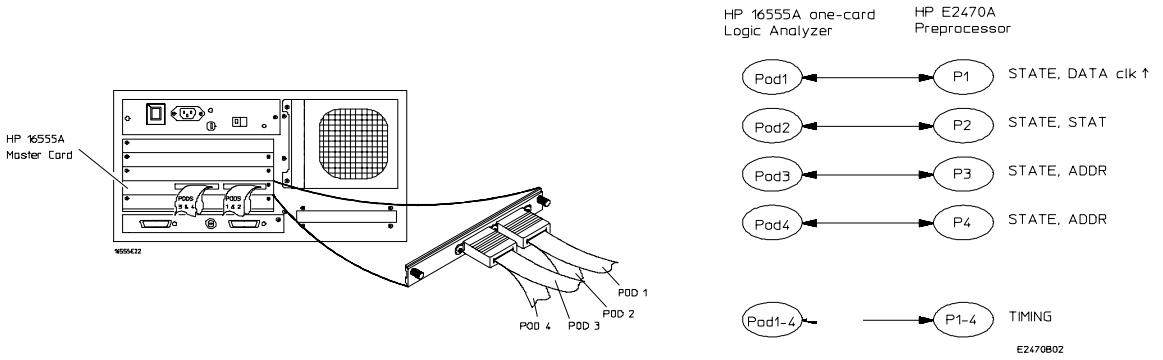
1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68HC16S. For **timing**, load configuration file F68HC16T.

To connect to the HP 16554A/55A/56A analyzer

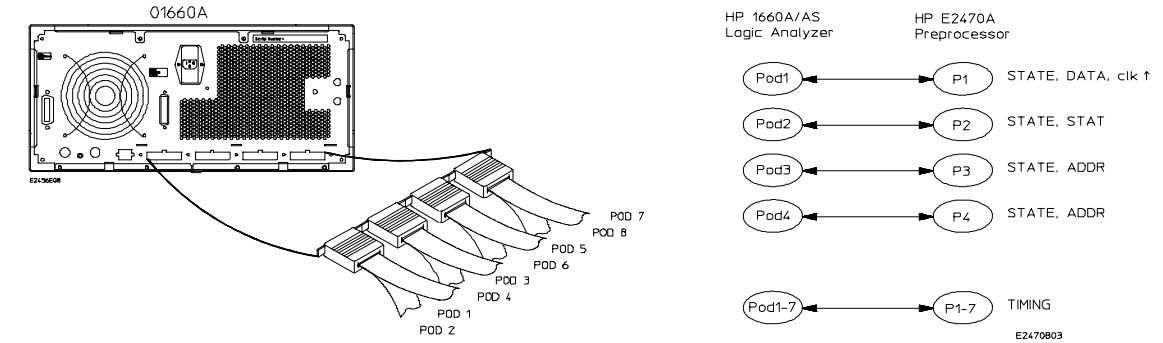
1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file M68HC16S. For **timing**, load configuration file M68HC16T.

To connect to the HP 1660A/AS analyzer

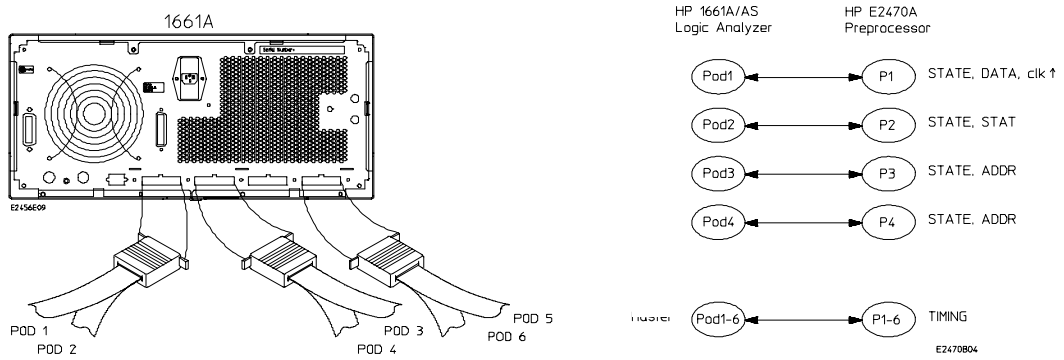
1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68HC16S. For **timing**, load configuration file F68HC16T.

To connect to the HP 1661A/AS analyzer

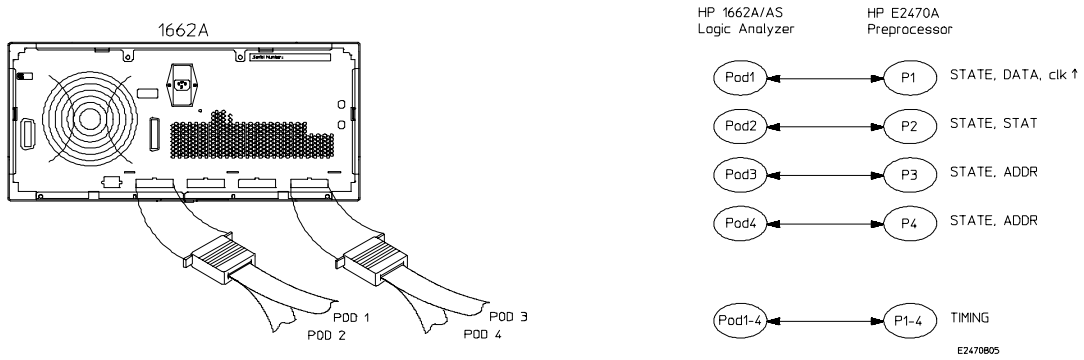
1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68HC16S. For **timing**, load configuration file F68HC16T.

To connect to the HP 1662A/AS analyzer

1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68HC16S. For **timing**, load configuration file F68HC16T.

Loading the Preprocessor Interface Software

The logic analyzer can be configured for MC68HC16Y1 analysis by loading the appropriate configuration file. Loading the state file automatically loads the inverse assembler file.

To load the configuration and inverse assembler

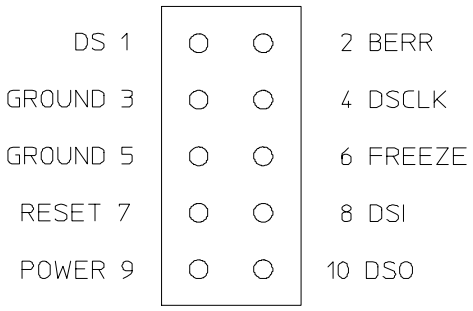
1. Make a duplicate copy of the master disk prior to setting up the preprocessor interface.
2. Insert the HP E2470A disk in the front disk drive of the logic analyzer.
3. Depending on your logic analyzer, select one of the following menus:
   - For the HP 1660-series logic analyzers, select the "System Disk" menu
   - For the HP 16500A mainframe, select the "System Front Disk" menu
   - For the HP 16500B mainframe, select the "System Flexible Disk" menu
4. Configure the menu to "Load" the analyzer configuration from disk.
5. Select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
6. Use the knob to select the appropriate configuration file.

   Choosing the correct configuration file depends on which analyzer you are using and whether you need timing or state analysis. The file names are listed at the bottom of the illustrations showing the connections for your particular logic analyzer.
7. Execute the load operation to load the file into the logic analyzer.

To connect to the Background Debug Monitor interface

The background debug monitor (BDM) interface allows an external controller to connect to and control the microcontroller through the preprocessor. The 10-pin BDM connector is defined in the figure below.

The BDM hardware is external to the preprocessor and may need to be supplied with voltage (either 5V or 3.3V) from the preprocessor or the target. The 3-pin connector (J2) allows the user to select the supply voltage sent to the BDM interface. If the 2-pin jumper is connected between pins 1 and 2, 5V is connected. If the jumper is connected between pins 2 and 3, the voltage of the MC68HC16Y1 is connected. It is assumed that if the BDM hardware is operating at 3.3V the MC68HC1 s also a 3.3V device. If, however, the MC68HC16Y1 is a 5V device and the BDM hardware is 3.3V, the jumper may be removed and a 3.3V source may be attached to pin 2 of J2.



Background Debug Interface

Analyzing the Motorola MC68HC16Y1

Analyzing the Motorola MC68HC16Y1

This chapter describes preprocessor interface data, symbol encodings, and information about the available inverse assemblers.

Displaying Information

This section describes how to display analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

To display the format specification

- **Select the format specification menu for your logic analyzer.**

  The configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microcontroller and any coprocessors connected directly to the microcontroller.

  The figure below shows the Format specification for state analysis. The figure on the following page shows the Format specification for timing analysis.

  Chapter 3 of this guide contains a table that lists the signals for the MC68HC16Y1 processor and on which pod and probe bit the signal comes into the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the processor signals should be on the format specification screen.

Figure 5

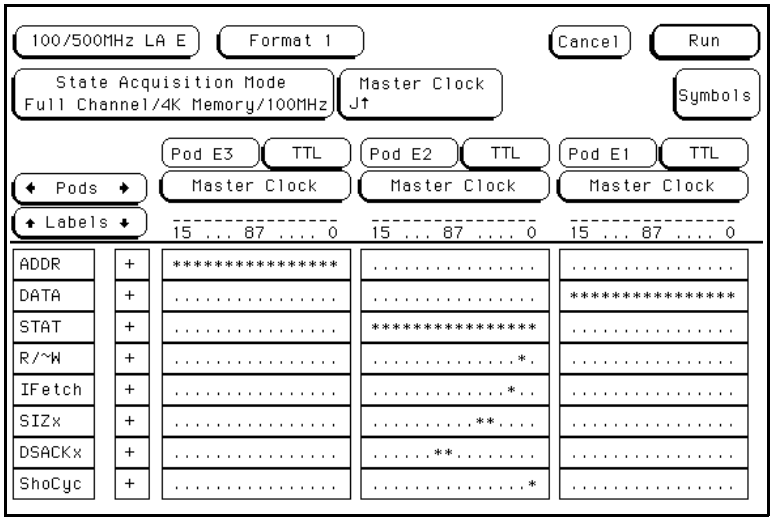
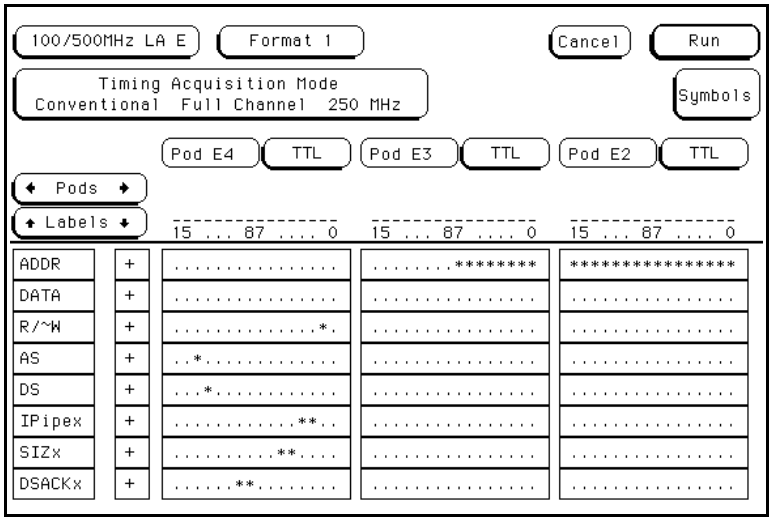


Figure 6



Additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.

Do you want any screen shots?

To display the configuration labels and symbols

- Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.

  The HP E2470A configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific MC68HC16Y1 cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

Table 2-1 MC68HC16Y1 Status Bit Definition

Bit	Status Signal	Description
0	~SHOW_CYCLE	Indicates an internal MCU cycle.
1	Rd/~Wr	Indicates the direction of data transfer.
2	~INST_FETCH	Indicates an instruction fetch.
3	~PIPE_FLUSH	Indicates an instruction caused an instruction pipeline flush.
4, 5	SIZE0/1	Indicates the number of bytes in a transfer.
6	~SIZE0_VALID	Indicates that the MCU is configured to supply SIZE0.
7	~SIZE1_VALID	Indicates that the MCU is configured to supply SIZE1.
8, 9	~DSACK0/1	Indicates the number of bytes accepted/provided in a transfer.
10	~BERR	Indicates a bus error for a particular cycle.
11	~BUS_CONTROL_INVALID	Indicates that the MCU is not configured to supply ~BR, ~BA, and ~BGACK.
12	~FCx_INVALID	Indicates that the MCU is not configured to supply FC0, FC1, AND FC2.
13	~A19_THRU_A23_INVALID	Indicates that the MCU is not configured to supply A19-A23.
14	FREEZE	When asserted, indicates the MCU is operating in background mode. When negated, indicates normal mode.
15	~BKPT	When asserted, indicates the MCU has encountered a hardware breakpoint.

Table 2-2 MC68HC16Y1 Symbolic Representation of Status Bits

Label	Symbol	Status Encoding
Cycle Type	**Opcode Fetch**	
	(internal)	x x x 2 H or x x x A H
	(external)	x x x 3 H or x x x B H
	Data Read	
	(internal)	x x x 6 H or x x x E H
	(external)	x x x 7 H or x x x F H
	Data Write	
	(internal)	x x x 4 H or x x x C H
	(external)	x x x 5 H or x x x D H
Size of Transfer		
	Byte Transfer (8 bit)	x x 1 x H
	Word Transfer (16 bit)	x x 2 x H
	3-Byte Transfer (24 bit)	x x 3 x H
	Long Word Transfer (32 bit)	x x 0 x H

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when specifying a trigger condition or a storage qualification that follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microcontroller only prefetches at most two words, one technique to avoid unwanted triggering from unused prefetches is to add "4" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

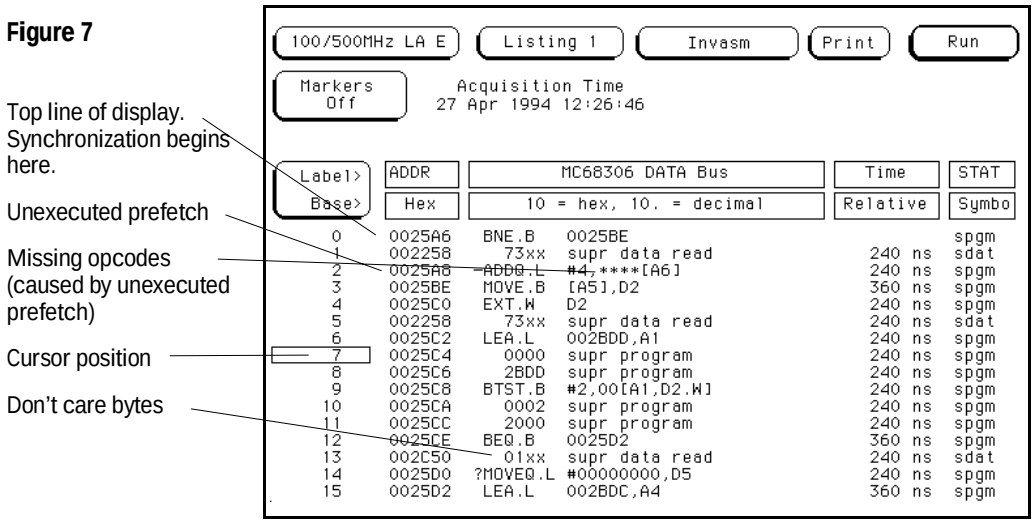
To display captured state data

- **Select the Listing Menu for your logic analyzer.**
  The logic analyzer displays captured data in the Listing Menu. The inverse assembler disassembles the captured data in a format that closely resembles the assembly source code for your processor.

Example

The following figure shows the Listing Menu display for the HP 16550A logic analyzer:

Figure 7



This section discusses the general output format of the inverse assembler and controller-specific information. This section also assumes that an inverse assembler has been loaded.

General Output Format

The next few paragraphs describe the general output format of the inverse assembler.

Numeric Format

Unless a value is followed by a suffix character, numeric output from the inverse assembler is in hexadecimal format. For example, decimal values have a period (.) as the suffix character; binary values have a percent sign (%) prefix.

Missing Opcodes/Operands

Asterisks (*) in the inverse assembler output indicate missing operands. Missing operands occur frequently and are primarily due to microcontroller prefetch activity. Storage qualification or the use of storage windows can also lead to such occurrences.

Don't Care Bytes

The MC68HC16Y1 microcontroller can perform 3-byte transfers. During operand reads and writes, 16-bit (word) values appear on the microcontroller data bus lines. The inverse assembler will attempt to display "xx" for any byte in a transfer that is ignored by the microcontroller. You can then determine exactly which byte or bytes of data were used as an operand. If the microcontroller is configured such that the number of bytes being transferred cannot be determined, an entire word will be displayed. The user must then determine which byte(s) is valid.

Unexecuted Prefetched Instructions

Prefetched instructions which are not executed by the microcontroller are marked by a hyphen "-" in the first column of the mnemonic/hex field.

Controller Specific Information

This section discusses issues specific to the MC68HC16Y1 inverse assembler including NON-MCU activity indicators.

Acquisitions of coprocessor and background cycles may be individually enabled/disabled via the slide switches on the preprocessor.

A "c" marks coprocessor activity and background activity is marked with a "b". The "c" and "b" are displayed in the first column of the mnemonic/hex field.

General Missing Terms

Depending on the configuration of the microcontroller, the inverse assembler may be unable to supply all of the information it normally supplies. For example, if ~DS (data strobe) is not valid, internal cycles cannot be captured. Additionally, if the function control pins FC0, 1, and 2 are configured as chip selects, the "user" and "supr" memory space indicator terms will not be displayed.

Filtering

The MC68HC16Y1 inverse assembler is capable of suppressing certain acquired bus cycles from the display thus allowing the user to focus on and display cycles of interest. The filter softkeys are part of the "Invasm Options" submenu. "Invasm Options" must be pressed to display the submenu.

Cycle suppression is broken down into the following categories: extension words, unexecuted prefetches, branches, calls and returns, other instructions, data reads, and data writes.

Extension words and unexecuted fetches are suppressed without regard to user mode or supervisor mode because they do not affect the display of executed mnemonics.

All other categories may be suppressed based on the user mode, supervisor mode, or both. These categories suppress actual executed mnemonics for the display.

Controller Configurations

The E2470A preprocessor interface and inverse assembler will support any MC68HC16Y1 configuration except those that use a Port C signal as a general purpose input/output.

To use the inverse assembly options

The Inverse Assembly Options menu contains two functions: display filtering with Show/Suppress selections, and Code Synchronization. To access the Inverse Assembly Options menu, press the Invasm Options softkey at the top of the screen.

Show/Suppress

The Show/Suppress settings determine whether certain classes of acquisition states are shown or suppressed on the logic analyzer display. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether the acquired data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, I/O branches can be shown, with all other operations suppressed, allowing quick analysis of I/O branch flow.

Note: If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microcontroller code (see next section).

To synchronize the inverse assembler

- Identify a line on the display that you know is the first state of an instruction fetch.
- Roll this line to the top of the listing.
- Press the Invasm Options softkey at the top of the screen.

  This will cause the Invasm Options submenu to appear.
- Press the Align softkey.

  The listing will inverse assemble from the top line down. Any data before this screen is left unchanged. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the listing by entering a new line number or by rolling the screen down, you may have to re-synchronize the inverse assembler by repeating the described steps.

  Each time you inverse assemble a block of memory, the analyzer will keep the alignment information for that block. Pressing the Align key clears the alignment information from the top of the screen to the end of the acquisition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Inverse assembler error messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Fatal Data Error

Displayed if the trace memory could not be read properly on entry into the inverse assembler.

Illegal Opcode <code>

Displayed if the inverse assembler encounters an illegal instruction.

Reserved Opcode

Displayed if the inverse assembler encounters a reserved coprocessor instruction.

Incomplete Opcode

Displayed if the inverse assembler cannot acquire all words of a multi-word instruction.

***s**

Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the HP E2470A hardware including product, electrical, and environmental characteristics, signal mapping, a brief theory of operation, circuit board dimensions, and repair information.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Product Characteristics

Microcontroller Supported	Motorola 68HC16Y1
Package Supported	160-pin PQFP for 68HC16Y1
Logic Analyzer Required	HP 1660A/61A/62A, HP 16550A, HP 16554A, HP 16555A, or HP 16556A.
Probes Required	Mandatory 4 for state. Up to 7 for timing.
Accessories Required	HP E5335A Probe Adapter One 01650-63203 Termination Adapter for each pod used for timing measurements, or the GP (General Purpose) probes supplied with your logic analyzer.

Electrical Characteristics

Power Requirements	250 mA typical @ 5 V, supplied by logic analyzer.	
Signal Line Loading	8 pF maximum on all signals except CLKOUT which has 40 pF maximum.	

Environmental Characteristics

Temperature	Operating	0 to + 55 degrees C +32 to +131 degrees F
	Nonoperating	-40 to + 75 degrees C -40 to +167 degrees F
Altitude	Operating	4,600 m 15,000 feet
	Nonoperating	15,300 m 50,000 feet
Humidity	Up to 90% noncondensing. Avoid sudden , extreme temperature changes which could cause condensation on the circuit board.	

Theory of Operation and Clocking

For timing measurements, raw digital signals from the MC68HC16Y1 are presented to the logic analyzer through the timing connectors. The acquisition clock is provided by the logic analyzer.

For state measurements, raw digital signals from the MC68HC16Y1 and generated signals from the programmable logic are latched and presented to the logic analyzer through the state connectors. The acquisition clock is generated by the programmable logic.

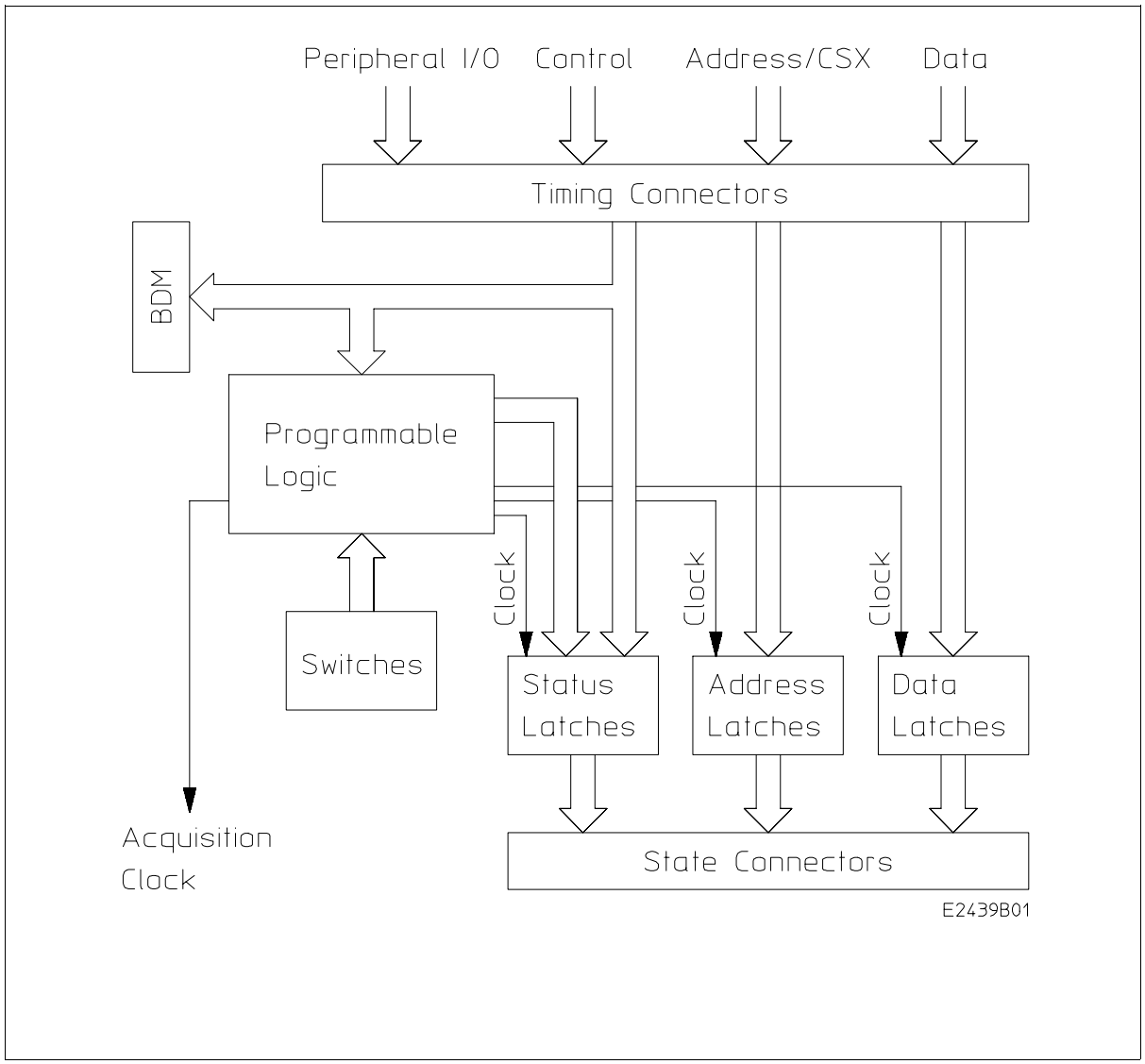
As can be seen in the timing diagram on page 3-6, all state information (data, address, and status) for external cycles (normal and fast termination) is available within the bus cycle. For internal cycles (also known as show cycles), however, data is not available until after the completion of the bus cycle. To capture both internal and external cycles with a single acquisition clock, all timing must conform to the internal cycle case. The acquisition clock must be delayed until a clock after any bus cycle completes. In turn, all state information must be latched.

Signals that could be used in address calculations, including address, chip selects, and function codes, are latched at the same time. Although bus control signals could be active and latched with this group, BGACK is the only signal of importance and, if asserted, prevents the microcontroller from controlling the bus.

Status signals are latched at the end of the bus cycle and at the same time to minimize logic. While most status signals are valid much sooner, BERR and BKPT are valid only at the end.

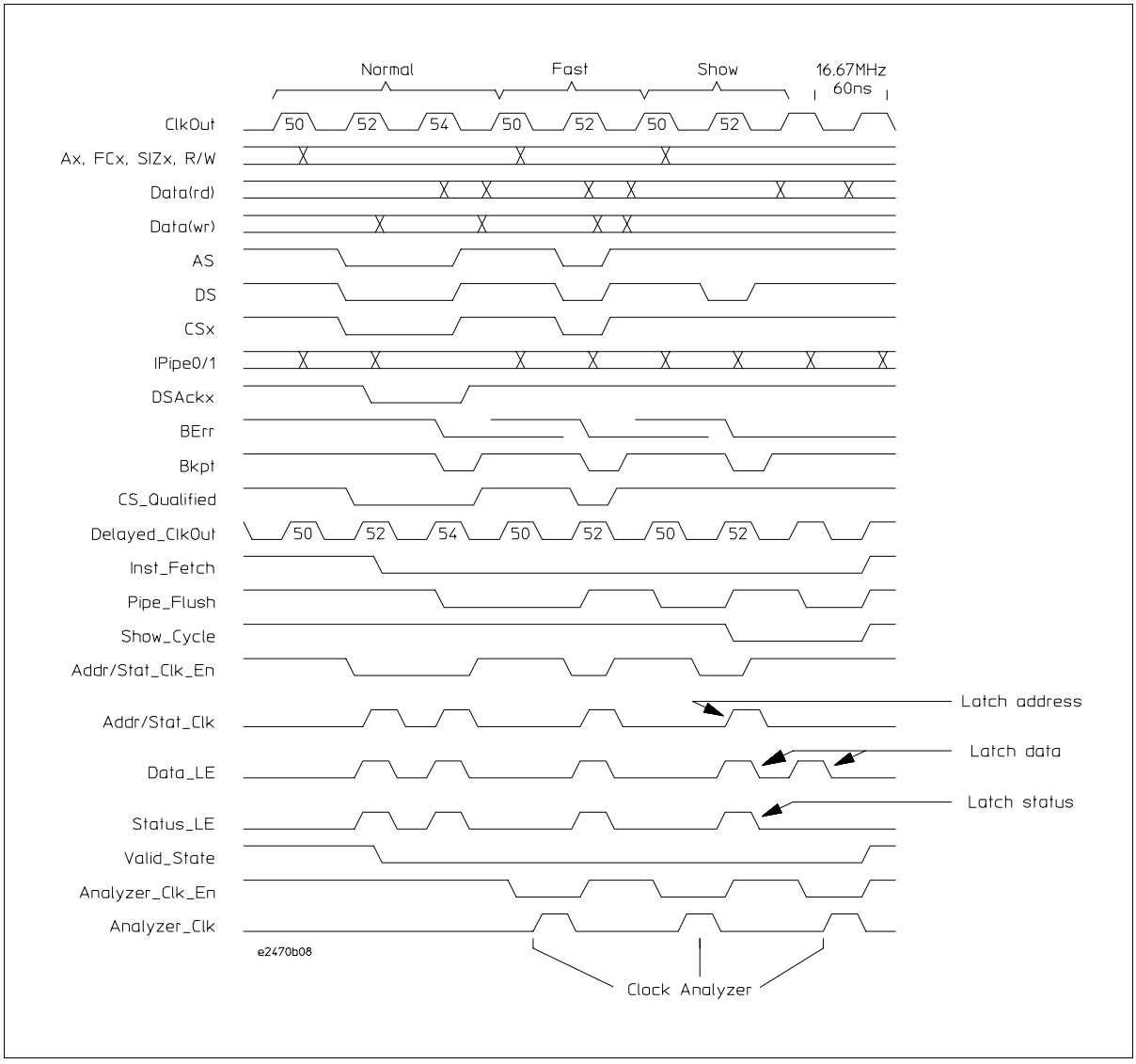
Data must be latched separately because it becomes valid at two different times.

The acquisition clock is always generated one clock after the end of a bus cycle. For address and status, and data on external cycles, this simply means extra set-up time. For internal cycles, it means that data is aligned with its associated address and status. Any combination of state signals may be specified in the trigger menu to find either an internal or external cycle.



Block Diagram

The following timing diagram shows the time at which address and data are sampled.



Timing Diagram

Signal-to-Connector Mapping

The following tables shows the preprocessor PGA socket pin mapping and the electrical interconnections implemented with the preprocessor interface. Table 3-1 is the HP E2470A State pod list. Table 3-2 is the HP E2470A Timing pod list. Table 3-3 is the MC68HC16Y1 signal to HP E2470A PGA connector list. The "Shield" signal is connected to the preprocessor interface ground but does not correspond to any particular MC68HC16Y1 GND pin.

State Connector Signal Definition

The following table defines the state connectors, the logic analyzer bit assignments, and the label/sublabel(s) to which a signal belongs. This table aids in reconfiguring the logic analyzer to match a particular microcontroller configuration.

TABLE 3-1 E2470A State Connector Signal List

SIGNAL NAME	E2470A STATE CONNECTOR PIN	ANALYZER BIT	STATE LABEL	STATE SUBLABEL	STATE SUBLABEL
DATA0	1-37	1- 0	DATA		
DATA1	1-35	1- 1	DATA		
DATA2	1-33	1- 2	DATA		
DATA3	1-31	1- 3	DATA		
DATA4	1-29	1- 4	DATA		
DATA5	1-27	1- 5	DATA		
DATA6	1-25	1- 6	DATA		
DATA7	1-23	1- 7	DATA		
DATA8	1-21	1- 8	DATA		
DATA9	1-19	1- 9	DATA		
DATA10	1-17	1-10	DATA		
DATA11	1-15	1-11	DATA		
DATA12	1-13	1-12	DATA		
DATA13	1-11	1-13	DATA		

SIGNAL NAME	E2470A STATE CONNECTOR PIN	ANALYZER BIT	STATE LABEL	STATE SUBLABEL	STATE SUBLABEL
DATA14	1- 9	1-14	DATA		
DATA15	1- 7	1-15	DATA		
ADDR0	3-37	3- 0	ADDR		
ADDR1	3-35	3- 1	ADDR		
ADDR2	3-33	3- 2	ADDR		
ADDR3	3-31	3- 3	ADDR		
ADDR4	3-29	3- 4	ADDR		
ADDR5	3-27	3- 5	ADDR		
ADDR6	3-25	3- 6	ADDR		
ADDR7	3-23	3- 7	ADDR		
ADDR8	3-21	3- 8	ADDR		
ADDR9	3-19	3- 9	ADDR		
ADDR10	3-17	3-10	ADDR		
ADDR11	3-15	3-11	ADDR		
ADDR12	3-13	3-12	ADDR		
ADDR13	3-11	3-13	ADDR		
ADDR14	3- 9	3-14	ADDR		
ADDR15	3- 7	3-15	ADDR		
ADDR16	4-37	4- 0	ADDR		
ADDR17	4-35	4- 1	ADDR		
ADDR18	4-33	4- 2	ADDR		
ADDR19/~CS6	4-31	4- 3	ADDR	CSx	
ADDR20/~CS7	4-29	4- 4	ADDR	CSx	
ADDR21/~CS8	4-27	4- 5	ADDR	CSx	
ADDR22/~CS9	4-25	4- 6	ADDR	CSx	
ADDR23/~CS10	4-23	4- 7	ADDR	CSx	
~CSBOOT	4-21	4- 8	ADDR_B	CSx	
~BR/~CS0	4-19	4- 9	ADDR_B	BusArb	CSx
~BG/~CSM	4-17	4-10	ADDR_B	BusArb	CSx
~BGACK/~CSE	4-15	4-11	ADDR_B	BusArb	CSx
FC0/~CS3	4-13	4-12	ADDR_B	FCx	CSx
FC1	4-11	4-13	ADDR_B	FCx	CSx

SIGNAL NAME	E2470A STATE CONNECTOR PIN	ANALYZER BIT	STATE LABEL	STATE SUBLABEL	STATE SUBLABEL
FC2/~CS5	4- 9	4-14	ADDR_B	FCx	CSx
unused	4- 7	4-15			
~SHOW_CYCLE	2-37	2- 0	STAT	ShoCyc	
R/~W	2-35	2- 1	STAT	R/~W	
~INST_FETCH	2-33	2- 2	STAT	IFetch	
~PIPE_FLUSH	2-31	2- 3	STAT	PFlush	
SIZ0	2-29	2- 4	STAT	SIZx	
SIZ1	2-27	2- 5	STAT	SIZx	
~SIZE0_VALID	2-25	2- 6	STAT		
~SIZE1_VALID	2-23	2- 7	STAT		
QUALIFIED_ DSACK0	2-21	2- 8	STAT	DSACKx	
QUALIFIED_ DSACK1	2-19	2- 9	STAT	DSACKx	
~BERR	2-17	2-10	STAT	BErr	
~BUS_ARB_ INVALID	2-15	2-11	STAT		
~FCx_INVALID	2-13	2-12	STAT		
~A19-A23_ INVALID	2-11	2-13	STAT		
FREEZE/QUOT	2- 9	2-14	STAT	Freeze	
~BKPT/DSCLK	2- 7	2-15	STAT	Bkpt	

Timing Connector Signal Definition

The following table defines the timing connectors, the logic analyzer bit assignments, and the label to which a signal belongs.

Table 3-2 E2470A Timing Connector Signal List

SIGNAL NAME	E2470A TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
DATA0	1-19	1- 0	DATA
DATA1	1-18	1- 1	DATA
DATA2	1-17	1- 2	DATA
DATA3	1-16	1- 3	DATA
DATA4	1-15	1- 4	DATA
DATA5	1-14	1- 5	DATA
DATA6	1-13	1- 6	DATA
DATA7	1-12	1- 7	DATA
DATA8	1-11	1- 8	DATA
DATA9	1-10	1- 9	DATA
DATA10	1- 9	1-10	DATA
DATA11	1- 8	1-11	DATA
DATA12	1- 7	1-12	DATA
DATA13	1- 6	1-13	DATA
DATA14	1- 5	1-14	DATA
DATA15	1- 4	1-15	DATA
ADDR0	2-19	2- 0	ADDR
ADDR1	2-18	2- 1	ADDR
ADDR2	2-17	2- 2	ADDR
ADDR3	2-16	2- 3	ADDR
ADDR4	2-15	2- 4	ADDR
ADDR5	2-14	2- 5	ADDR
ADDR6	2-13	2- 6	ADDR
ADDR7	2-12	2- 7	ADDR
ADDR8	2-11	2- 8	ADDR
ADDR9	2-10	2- 9	ADDR

SIGNAL NAME	E2470A TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
ADDR10	2- 9	2-10	ADDR
ADDR11	2- 8	2-11	ADDR
ADDR12	2- 7	2-12	ADDR
ADDR13	2- 6	2-13	ADDR
ADDR14	2- 5	2-14	ADDR
ADDR15	2- 4	2-15	ADDR
ADDR16	3-19	3- 0	ADDR
ADDR17	3-18	3- 1	ADDR
ADDR18	3-17	3- 2	ADDR
ADDR19/~CS6	3-16	3- 3	ADDR
ADDR20/~CS7	3-15	3- 4	ADDR
ADDR21/~CS8	3-14	3- 5	ADDR
ADDR22/~CS9	3-13	3- 6	ADDR
ADDR23/~CS10	3-12	3- 7	ADDR
~CSBOOT	3-11	3- 8	CSX
~BR/~CS0	3-10	3- 9	BUSARB
~BG/~CSM	3- 9	3-10	BUSARB
~BGACK/~CSE	3- 8	3-11	BUSARB
FC0/~CS3	3- 7	3-12	FCX
FC1	3- 6	3-13	FCX
FC2/~CS5	3- 5	3-14	FCX
unused	3- 4	3-15	
~AVEC	4-19	4- 0	AVEC
R/~W	4-18	4- 1	R/~W
PIPE1/DSI	4-17	4- 2	IPIPEx
PIPE0/DSO	4-16	4- 3	IPIPEx
SIZ0	4-15	4- 4	SIZx
SIZ1	4-14	4- 5	SIZx
~RESET	4-13	4- 6	RESET
~HALT	4-12	4- 7	HALT
~DSACK0	4-11	4- 8	DSACKx
~DSACK1	4-10	4- 9	DSACKx

SIGNAL NAME	E2470A TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
~BERR	4- 9	4-10	BERR
PE3	4- 8	4-11	
~DS	4- 7	4-12	DS
~AS	4- 6	4-13	AS
FREEZE/QUOT	4- 5	4-14	FREEZE
~BKPT/DSCLK	4- 4	4-15	Bkpt
MISO	5-19	5- 0	PMC
RXDB	5-18	5- 1	PMC
MOSI	5-17	5- 2	PMC
TXDB	5-16	5- 3	PMC
SCK	5-15	5- 4	PMC
RXDA	5-14	5- 5	PMC
~SS	5-13	5- 6	PMC
TXDA	5-12	5- 7	IRQ
~IntReq7	5-11	5- 8	IRQ
~IntReq6	5-10	5- 9	IRQ
~IntReq5	5- 9	5-10	IRQ
~IntReq4	5- 8	5-11	IRQ
~IntReq3	5- 7	5-12	IRQ
~IntReq2	5- 6	5-13	IRQ
~IntReq1	5- 5	5-14	IRQ
ModClk	5- 4	5-15	ModClk
PGP0/IC1	6-19	6- 0	PGP
PGP1/IC2	6-18	6- 1	PGP
PGP2/IC3	6-17	6- 2	PGP
PGP3/OC1	6-16	6- 3	PGP
PGP4/OC2/OC1	6-15	6- 4	PGP
PGP5/OC3/OC1	6-14	6- 5	PGP
PGP6/OC4/OC1	6-13	6- 6	PGP
PGP7/IC4/OC5/OC1	6-12	6- 7	PGP
not used	6-11	6- 8	
PWMA	6-10	6- 9	PWMA

SIGNAL NAME	E2470A TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
PWMB	6- 9	6-10	PWMB
PAI	6- 8	6-11	PAI
PClk	6- 7	6-12	PClk
T2Clk	6- 6	6-13	T2Clk
TSC	6- 5	6-14	TSClk
ClkOut	6- 4	6-15	ClkOut
TP0	5-19	5- 0	TPU
TP1	5-18	5- 1	TPU
TP2	5-17	5- 2	TPU
TP3	5-16	5- 3	TPU
TP4	5-15	5- 4	TPU
TP5	5-14	5- 5	TPU
TP6	5-13	5- 6	TPU
TP7	5-12	5- 7	TPU
TP8	5-11	5- 8	TPU
TP9	5-10	5- 9	TPU
TP10	5- 9	5-10	TPU
TP11	5- 8	5-11	TPU
TP12	5- 7	5-12	TPU
TP13	5- 6	5-13	TPU
TP14	5- 5	5-14	TPU
TP15	5- 4	5-15	TPU

PQFP to PGA Connector Signal Definition

The following table defines the 68HC16Y1 pins and the corresponding pins on the HP E2470A PGA socket. For those signals that are also connected to a Timing pod, the Timing pod number is shown.

TABLE 3-3 Probing Signal List

68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
1	VRH		C2	
2	PADA5/AN5		D1	
3	PADA4/AN4		D2	
4	PADA3/AN3		D3	
5	PADA2/AN2		D4	
6	PADA1/AN0		D5	
7	PADA0/AN1		E1	
8	VSSA		E2	
9	VDDA		E3	
10	VDDE1		E4	
11	VSSE1	X	E5	
12	ADDR1		F1	2
13	ADDR2		F2	2
14	ADDR3/PB0		F3	2
15	ADDR4/PB1		F4	2
16	ADDR5/PB2		F5	2
17	ADDR6/PB3		G1	2
18	ADDR7/PB4		G2	2
19	ADDR8/PB5		G3	2
20	ADDR9/PB6		G4	2
21	VSSI		G5	
22	ADDR10/PB10		G6	2
23	ADDR11/PA0		H1	2
24	ADDR12/PA1		H2	2
25	ADDR13/PA2		H3	2

68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
26	VDDE2		H4	
27	VSSE2	X	H5	
28	ADDR14/PA3		H6	2
29	ADDR15/PA4		J1	2
30	ADDR16/PA5		J2	3
31	ADDR17/PA6		J3	3
32	ADDR18/PA7		J4	3
33	~SS/PMC3		J5	5
34	MOSI/PMC1		J6	5
35	SCK/PMC0		K2	5
36	MISO/PMC2		K1	5
37	TXDA/PMC7		K3	5
38	RXDA/PMC6		L1	5
39	TXDB/PMC5		L2	5
40	VDDE4			
41	VSSE4	X		
42	RXDB/PMC4		P4	5
47	TPUCH0		N4	7
48	TPUCH1		M4	7
45	TPUCH2		L 4	7
46	TPUCH3		K 4	7
47	VDDE		L3	
48	VSSE	X	N 3	
49	TPUCH4		M 5	7
50	TPUCH5		L 5	7
51	TPUCH6		K5	7
52	TPUCH7		P 6	7
53	TPUCH8		N 6	7
54	TPUCH9		M 6	7
55	TPUCH10		L 6	7
56	TPUCH11		K 6	7

68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
57	VDDE			
58	VSSI			
59	TPUCH12		M 7	7
60	TPUCH13		L 7	7
61	TPUCH14		K 7	7
62	TPUCH15		J 7	7
63	T2CLK		P 8	6
64	nc		N 8	
65	VSTBY		M 8	
66	XTAL		L8	
67	VDOSYN		K 8	
68	EXTAL		J 8	
69	VSSI	X	P 9	
70	VDDI			
71	XFC		M9	
72	VDDE		P 5	
73	VSSI		P9	
74	CLKOUT		J9	
75	VSSE	X	P10	
76	~RESET		N10	4
77	~HALT		M10	4
78	~BERR		P11	4
79	FREEZ/QUOT		N11	4
80	TSC		M11	6
81	~IRQ7/PF7		M13	5
82	~IRQ6/PF6		L14	5
83	~IRQ5/PF5		L13	5
84	~IRQ4/PF4		L12	5
85	~IRQ3/PF3		L11	5
86	~IRQ2/PF2		L10	5
87	~IRQ1/PF1		K14	5
88	MODCLK/PF0		K13	5

68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
89	R/~W		K12	4
90	SIZ1/PE7		K10	4
91	SIZ0/PE6		K11	4
92	~AS/PE5		J14	4
93	~DS/PE4		J13	4
94	VSSE7	X	K11	
95	VDDE7		K10	
96	PE3		J10	4
97	~AVEC/PE2		H14	4
98	~DSACK1/PE1		H13	4
99	~DSACK0/PE0		H12	4
100	ADDR0		H11	2
101	VSSI		H10	
102	DATA15/PG7		H9	1
103	DATA14/PG6		G14	1
104	DATA13/PG5		G13	1
105	DATA12/PG4		G12	1
106	DATA11/PG3		G11	1
107	VSSE7	X	G10	
108	VDDE7		G9	
109	DATA10/PG2		F14	1
110	DATA9/PG1		F13	1
111	DATA8/PG0		F12	1
112	DATA7/PH7		F11	1
113	DATA6/PH6		F10	1
114	DATA5/PH5		F9	1
115	DATA4/PH4		E14	1
116	DATA3/PH3		E13	1
117	DATA2/PH2		E12	1
118	DATA1/PH1		D14	1
119	DATA0/PH0		D13	1
120	VDDE11		D12	
121	VSSE11	X		
122	~CSBOOT		A11	3

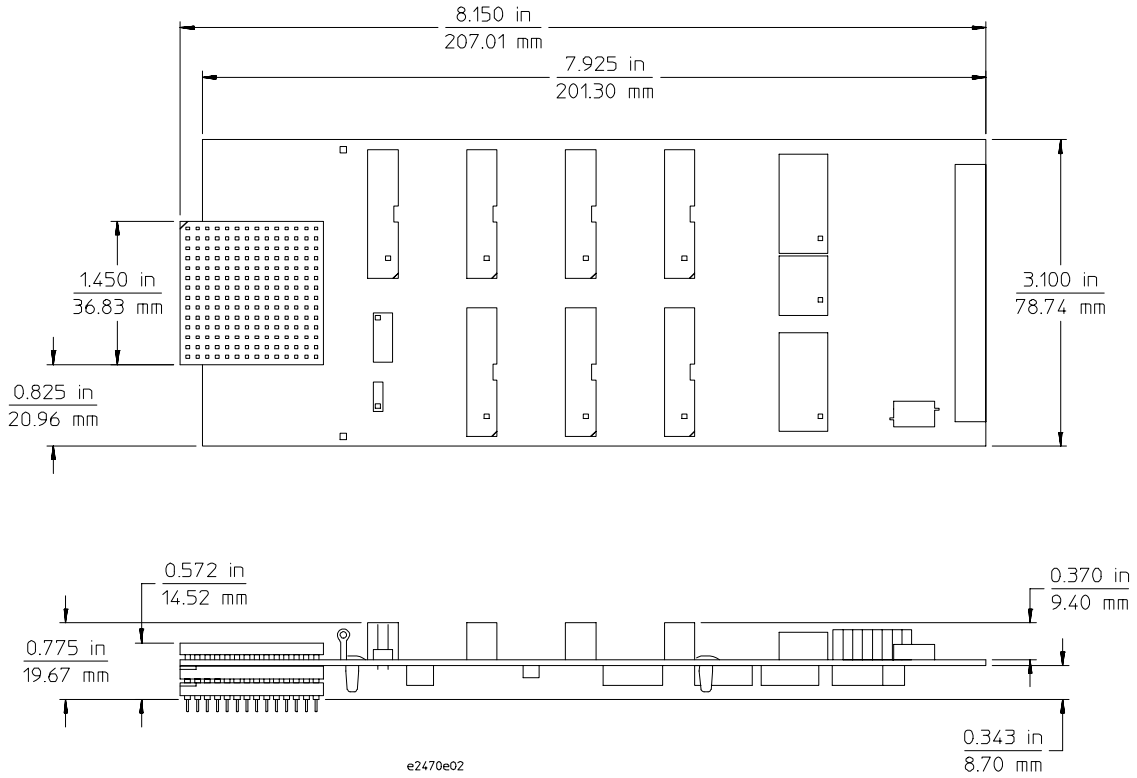
68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
123	~BR/~CS0		B11	3
124	~BG		C11	3
125	~BGACK/~CSE		D11	3
126	FC0/~CS3/PC0		E11	3
127	FC1/PC1		A10	3
128	FC2/~CS5/PC2		B10	3
129	VDDE10			
130	VSSE10	X		
131	ADDR19/~CS6/PC3		E10	3
132	ADDR20/~CS7/PC4		A9	3
133	ADDR21/~CS8 /PC5		B9	3
134	ADDR22/~CS9/PC6		C9	3
135	ADDR23/~CS10/PC7		D9	3
136	VDDI			
137	VSSI			
138	nc			
139	~BKPT/DSCLK		C8	4
140	PIPE0/DSO		E8	4
141	PIPE1/DSI		D8	4
142	VDDE11			
143	VSSE11	X		
144	PCLK		B7	6
145	PWMB		C7	6
146	PWMA		D7	6
147	PAI		E 7	6
148	IC4/OC5/OC1/PGP7		F 7	6
149	OC4/OC1/PGP6		A6	6
150	OC3/OC1/PGP5		B6	6
151	OC4/OC1/PGP4		C6	6
152	OC1/PGP3		D6	6
153	IC3/PGP2		E6	6
154	IC2P/GP1		F 6	6
155	IC1P/GP0		A5	6
156	VDDE12			

68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
157	VSSE12	X		
158	PADA7/AN7		A4	
159	PADA6/AN6		B4	
160	VRL		C4	
		shield	A 1	
		shield	A 2	
		shield	A 3	
		shield	A12	
		shield	A13	
		shield	A14	
		shield	B 1	
		shield	B 2	
		shield	B 3	
		shield	B13	
		shield	B14	
		shield	C 1	
		shield	C 3	
		shield	C12	
		shield	C13	
		shield	C14	
		shield	M 1	
		shield	M 2	
		shield	M 3	
		shield	M12	
		shield	M14	
		shield	N 1	
		shield	N 2	
		shield	N12	
		shield	N13	
		shield	N14	
		shield	P 1	
		shield	P 2	
		shield	P 3	
		shield	P12	

68HC16Y1 PIN	68HC16Y1 SIGNAL NAME	SYSTEM GROUND	E2470A PGA PIN	E2470A TIMING POD
		shield	P13	
		shield	P14	

Circuit Board Dimensions

The following figure gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.



Dimensions

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Table 3-3 Replaceable Parts

HP Part Number	Description
E2470-69501	Circuit board assembly
E2470-68701	Inverse assembler disk pouch
E5335A	160-pin PQFP to generic PGA

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Target System Problems

This section lists problems that you might encounter with the target system. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the logic analyzer, the microprocessor (if socketed) or the cables may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the logic analyzer and target system.**

  1 Power up the analyzer.

  2 Power up the target system.

  If you power up the target system before you power up the logic analyzer, interface circuitry may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the cables are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the target system and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- **Do a full reset of the target system before beginning the measurement.**

  Some designs require a full reset to ensure correct configuration.

- **Ensure that your target system meets the timing requirements with the logic analyzer probe connected.**

  See "Capacitive Loading" in this chapter. While logic analyzer loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- **Ensure that you have sufficient cooling for the microprocessor.**

  Microprocessors such as the i486, Pentium™, and MC68040 generate substantial heat. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the logic analyzer, or system lockup in the microprocessor. All interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- **Remove as many pin protectors, extenders, and adapters as possible.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- **Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the cursor position) and pressing the Invasm key.**

  The inverse assembler works from the first line of the trace *display.* If you jump to the middle of a trace and select Invasm, prior trace states may not be disassembled correctly. If you move to several random places in the trace list and synchronize the disassembly each time, the trace disassembly is only guaranteed to be correct for the portion of the trace list disassembled. See "To synchronize the inverse assembler" in Chapter 2 for more information.

- **Ensure that each logic analyzer pod is connected to the correct connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and connector numbers. Target systems must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each connector are often altered to support that need. Thus, one target system might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**
- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  Except in certain cases (see page 1-7), these labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some preprocessors also require other data labels. See Chapter 2 for more information.
- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.
- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler or rename it, the configuration process will fail to load the disassembler.

  See Chapter 1 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope may miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted, and that it is located on the smae flexible disk or in the same directory as the configuration file.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for one or two HP 16550A logic analysis cards. Ensure that your cable connections match the silk screening on the card. Then, repeat the measurement.

See Also The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.

- If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

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About this edition

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The following list of pages gives the date of the current edition and of any changed pages to that edition.

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	Yes	No
1. Did you receive your product when expected?	[ ]	[ ]
2. Were you satisfied with the operation of the instrument at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

If not, what was missing?

Probes [ ] Manual(s) [ ] Other _____

4. What measurements will this instrument be used to make? _____

_____

5. How will the instrument be controlled?

Front Panel [ ] HP-IB [ ] RS-232C [ ] Controller Type _____

6. What do you like most about the instrument? _____

_____

_____

7. What would you like to see changed or improved? _____

_____

_____

8. Which manuals have you used?

[ ] User's Guide
[ ] User's Reference
[ ] Programmer's Guide
[ ] Service Guide

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[ ] Breadth and depth of information
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Please explain: _____

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